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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,472	03/30/2001	Thomas E. Willis	42390.P8930	6094

8791 7590 09/22/2005

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EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,472	WILLIS ET AL.	
	Examiner	Art Unit	
	Gary J. Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30 and 35-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30 and 35-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/08/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 and 35-46 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-30 and 35 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1, 9, 13, 20, and 35 substantially recite identifying if a virtual address translation is sharable transparent to the operating system. The disclosure shows sharing indications 1) at 616-618 of Fig. 6, or 2) at 705 and 706 of Figs. 7a and 7b. These sharing indications are compared with an input in order to determine if the input comes from a processor that is allowed to share the translation (specification pg. 14 lines 7-11, pg. 18 lines 14-17). The only mechanism shown for this is in Fig. 8 at PID (described at page 21 paragraph 0052). Since this PID is disclosed as a logical processor (Figs. 1-3), it is not necessarily generated by hardware, but rather may be set by the process or by some other software mechanism. How it is generated is apparently not disclosed. Applicant has stated that the operating system must be modified to support an equivalent process identifier such as in Bourekas (the arguments refuting the rejection over Bourekas, pgs. 7-9 of the brief). However, it has not been

shown how the present invention prevents the requirement to modify the operating system to set and submit the PID and thus how to make the identification of the sharability of the translation transparent to the operating system. In response to this rejection Applicant has stated that the generation of a PID is well known. Even if so, either the PID is set, generated and assigned by the OS and not transparent thereto, in both the application and in the cited prior art, or it is transparent to the OS in both the application and in the cited art. Since the present application is not clear on how this mechanism is transparent to the OS, it cannot be made by one of ordinary skill in the art without undue experimentation. Claims 2-8, 10-12, 14-19, and 21-30 depend from claims 1, 9, 13, and 20 respectively, and incorporate the limitations thereof.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-30 and 35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 9, 13, 20, and 35 substantially recite identifying if a virtual address translation is sharable transparent to the operating system. The disclosure appears to assign this substantially a negative limitation meaning; that is, it means *without requiring special operating system support or modifications* (page 7), or *without requiring the operating system to actively manage the sharing* (page 17). However, this definition does not adequately establish the metes and bounds desired by the claim language, since it is not clear what exactly is meant by "special support" and "actively manage", or whether either of both of these definitions

must be met. It is also not clear which operating system is referred to; for example the claims could hypothetically be rejected by simply finding any operating system that is not required to be modified or otherwise support or actively manage an address translation sharing indication (for example in another computer). In response to this rejection Applicant states that transparent means "a device or system that processes data without the user being aware of or needing to understand its operation". This response further clouds the issue, since it is not apparent whether Applicant intends this to mean as explained literally, or to mean "without the 'operating system' being aware of or need to understand its operation", and if so, whether this definition is intended instead of or in addition to the specification descriptions relevant to the term cited hereinabove. The meanings of "without being aware of or needing to understand its operation" (as argued), "without requiring support therefrom", "without requiring modifications thereto", and "without requiring active management thereby" (the last three as described in the specification) are all different. Claims 2-8, 10-12, 14-19, and 21-30 depend from claims 1, 9, 13, and 20 respectively, and incorporate the limitations thereof.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1-30 and 35-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Bourekas, U.S. Patent 6,598,050 B1, and (cited as evidenciary support) Tanebaum, "Modern Operating Systems".

8. As to claims 1-3, 5-10, and 12, Bourekas discloses a method, executable code, and processor for transparently sharing virtual address translations, by accessing a translation and identifying if it is sharable (see Abstract, Figs 1 and 2, col. 1 line 49 to col. 2 line 50, and col. 4 line 21 to col. 5 line 12; the global bit 115 explicitly and group membership fields 118 implicitly identify if the translation is sharable and if so by the current task, and this procedure is transparent to the OS as recited, since the prior art required OS traps but the invented system requires no traps and therefore no modification of or special support by the OS). This virtual address translation in general does not require OS support except during a page fault, the virtual address is supplied by the program/process and is translated by the hardware. See Tanenbaum, "Modern Operating Systems", where it is described that processes call the operating system using trap instructions (pgs. 16-19), that in paging in general a process generates a virtual address which is translated by the hardware and only requires an OS call upon a page fault (pgs. 89-92 and 105). It is therefore appears incorrect to state that the OS must be modified to support a group membership field with the virtual address, for any particular access request this is entirely supplied by the process, and the virtual address and group membership field comparisons are done in hardware (in the TLB of Bourekas, or if missed in a page table). However, it is certainly incorrect to state that

the OS must provide special support or actively manage the sharing of the translation, since it is not involved in routine translations (only at a page fault), and Bourekas further expressly states removing the requirement for trapping to the OS for the control of sharing translations.

9. As to claims 13-15, 19-22, and 28-30, Bourekas discloses processors and multiple logical processors as recited, since multiple tasks/processes are described.

10. As to claim 36, Bourekas discloses a multithreading processor comprising address translation stage with TLB 110 having plurality of entries to translate virtual to physical addresses (one entry shown in Fig. 1), first entry to translate a first virtual address for a first process, control logic comprising circuitry to identify sharability of the first entry (since a circuit must enter/read the G bit 115 to determine if the entry may be shared by all tasks) and to provide a first sharing indication if the first entry may be shared by a second process (since a circuit must enter/read the GRP field 118 and compare it with an incoming request field 107), and sharing indication field (at 118) in the first entry to store the first sharing indication (see Abstract, Figs 1 and 2, col. 1 line 49 to col. 2 line 50, and col. 4 line 21 to col. 5 line 12).

11. As to claims 24-27, 35, 40, and 42-46, Bourekas discloses that the TLB stores the indication (Fig. 1).

12. As to claims 4, 11, 37-38, and 41, in Bourekas the fields 118 identify the logical processes.

13. As to claims 23 and 29, Bourekas discloses the recited matching of second translation data to first since as shown in Fig. 4, multiple matches are performed which result in the recited identification of sharing.

14. As to claims 16-18, Bourekas discloses that the translations provide access to a shared cache, since as shown in Fig. 4 the translations whether to access main memory 238 or the cache 236, and the cache is shared since multiple tasks are performed in the depicted translation procedure.

15. As to claim 39, Bourekas discloses the comparison of the virtual address of any input process with the entries, and therefore inherently circuitry and state machine processes to the extent recited.

16. Claims 1-30 and 35-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Kakeda et al., U.S. Patent 6,564,311 B2.

17. As to claims 1-3, 5-10, and 12, Kakeda discloses a method, executable code, and processor for transparently sharing virtual address translations, by accessing a translation and identifying if it is sharable (see Abstract, Figs 1 and 2, col. 1 lines 10-15, col. 1 line 65 to col. 2 line 65, col. 4 lines 33-65, col. 5 lines 15-23 and 47-59, and col. 7 lines 1-10); the global bits 103 and PID 102 identify if the translation is sharable, and if so by the current task PID, and this procedure is transparent to the OS as recited, since the PID is supplied by the process in hardware 2 without regard to the virtual address, or the OS.

18. As to claims 13-15, 19-22, and 28-30, Kakeda discloses processors and multiple logical processors as recited, since multiple tasks/processes are described.

19. As to claim 36, Kakeda discloses a multithreading processor comprising address translation stage with TLB 1 having plurality of entries to translate virtual to physical addresses (entries shown at e1, etc., Fig. 1), first entry to translate a first virtual address for a first process, control logic comprising circuitry to identify sharability of the first entry (including 13 and 105, Fig. 1, 2) and to provide a first sharing indication if the first entry may be shared by a second process (since a circuit must enter as well as read the PID field 102 and compare it with an incoming request PID at 2), and sharing indication field 102 in the first entry to store the first sharing indication (see Abstract, Figs 1 and 2, col. 1 lines 10-15, col. 1 line 65 to col. 2 line 65, col. 4 lines 33-65, col. 5 lines 15-23 and 47-59, and col. 7 lines 1-10).

20. As to claims 24-27, 35, 40, and 42-46, Kakeda discloses that the TLB stores the indication (Fig. 1).

21. As to claims 4, 11, 37-38, and 41, in Kakeda the fields 118 identify the logical processes.

22. As to claims 23 and 29, Kakeda discloses the recited matching of second translation data to first since as shown in Fig. 4, multiple matches are performed which result in the recited identification of sharing.

23. As to claims 16-18, Kakeda discloses that the translations provide access to a shared cache, since as shown in Fig. 4 the translations whether to access main memory 238 or the cache 236, and the cache is shared since multiple tasks are performed in the depicted translation procedure.

24. As to claim 39, Kakeda discloses the comparison of the virtual address of any input process with the entries, and therefore inherently circuitry and state machine processes to the extent recited.

Response to Arguments

25. Applicant's arguments filed in the response of July 8, 2005 have been fully considered but they are not persuasive. Applicants respond to the 35 USC 112 P. 2 rejection by giving a computer science dictionary definition of "transparent" without stating whether this definition is intended as an addition to, or instead of, specification descriptions previously cited and questioned. Applicants state that examiner takes these phrases out of context, and in support of this statement cites a section that regards the ability to not require the OS in all cases to be transparent; however, the operation of the OS in cases where it is not transparent is not relevant to what the definition is of when the OS is operating transparently. Applicants argue that generation of a PID was well known in the art. Either the generation of the PID is not transparent to the OS (and thus the present invention cannot determine whether a translation may be shared by a particular processor ID transparently to the OS, and the 35 USC 112 P. 1 rejection holds), or the generation of the PID is transparent to the OS (and thus the cited art may identify whether a translation may be shared by a particular processor transparently to the OS, and the 35 USC 102 rejection holds). The specification sections cited as support of how the present invention is enabled do not mention that the translation is identified as sharable transparent to the OS.

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J. Portka whose telephone number is (571) 272-4211. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gary J Portka
Primary Examiner
Art Unit 2188

July 8, 2005

GARY PORTKA
PRIMARY EXAMINER